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2 What is claimed is:

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4 1. A system for channelizing an IF wideband input signal into  
5 separated channelized digital output signals, the system  
6 comprising,

7       a complex mixer for quadrature demodulation of the IF  
8 wideband input signal into a complex signal,

9       a polyphase clock generator for generating polyphase clock  
10 signals each having the same clocking signal that is staggered  
11 in phase over a clock cycle,

12       a parallel converter comprising a bank of samplers for  
13 respective sampling the complex signal into staggered sampled  
14 complex signals and comprising a bank of converters for  
15 converting the staggered sampled complex signals into  
16 respective sampled digital complex signals, each of the  
17 samplers of the bank of sampler sampling the complex signals at  
18 a rate of the clock cycle at a respective staggered phase, and

19       a parallel filter bank comprising a polyphase filter bank  
20 of filters for respective filtering the sampled digital complex  
21 signals into respective filtered complex signals and comprising  
22 a processor for transforming the filtered complex signals into  
23 the channelized digital output signals.

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2. The system of claim 1 wherein,

3       the processor is a Fast Fourier Transform processor for  
4 computing N point Fast Fourier transforms of the N filter  
5 complex signals once every clock cycle of  $(f_s/N)^{-1}$  seconds.

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7. The system of claim 1 wherein,

8       the polyphase filter bank comprises a plurality of digital  
9 filters each of which is a finite impulse response filter.

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11. The system of claim 1 wherein,

12       the polyphase filter bank comprises a plurality of digital  
13 filters each of which is an infinite impulse response filter.

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15. The system of claim 1 wherein,

16       the input signal comprises a plurality of channel signals  
17 that are frequency division multiple access signals having a  
18 channel bandwidth, and

19       the polyphase filter bank comprises a plurality of digital  
20 filters each of which having a bandwidth equal to 1/2 of a  
21 bandwidth of a respective channel signal in the input signal.

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2     6. The system of claim 1 wherein,  
3         the input signal is an IF wideband signal communicating  
4 channel signals communicated within a channel bandwidth,  
5         the complex signal comprises I and Q quadrature baseband  
6 signals,  
7         the staggered sampled complex signals are staggered  
8 sampled I and Q quadrature baseband signals,  
9         the sampled digital complex signals are digitized  
10 staggered sampled I and Q quadrature baseband signals,  
11         the filtered complex signals are baseband channel signals  
12 within 1/2 of the channel bandwidth, and  
13         the channelized digital output signals are separated  
14 baseband channel signals.

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1    7. A system for channelizing an IF wideband signal into  
2    channelized digital output signals, the system comprising,  
3        a complex mixer for quadrature demodulation of the IF  
4    wideband signal into a complex signal communicating channel  
5    signals communicated within a channel bandwidth, the complex  
6    signal comprises I and Q quadrature baseband signals,  
7        a polyphase clock generator for generating polyphase clock  
8    signals each of which having the same clocking signal that is  
9    staggered in phase over a clock cycle,  
10      a bank of samplers for respective sampling the I and Q  
11    baseband quadrature signals into staggered sampled I and Q  
12    quadrature signals, each of the samplers of the bank of sampler  
13    sampling the I and Q quadrature signals at a rate of the clock  
14    cycle at a respective staggered phase,  
15      a bank of converters for converting the staggered sampled I  
16    and Q quadrature signals into respective sampled digital I and  
17    Q quadrature signals,  
18      a polyphase filter bank of filters for respective  
19    filtering the sampled digital I and Q quadrature signals into  
20    respective filtered I and Q quadrature signals, and  
21      a processor for transforming the filtered I and Q  
22    quadrature signals into the channelized digital output signals.

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2   8. The system of claim 7 wherein,

3                 the processor is a Fast Fourier Transform processor for  
4 computing N point Fast Fourier transforms of the N filter  
5 complex signals once every clock cycle of  $(f_s/N)^{-1}$  seconds, and  
6                 the polyphase filter bank comprises a plurality of digital  
7 filters each of which is a finite impulse response filter.

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9   9. The system of claim 7 wherein,

10                the IF wideband signal comprises a plurality of channel  
11 signals that are in frequency division multiple access signals  
12 having a channel bandwidth, and

13                the polyphase filter bank comprises a plurality of digital  
14 filters each of which having a bandwidth equal to 1/2 of a  
15 bandwidth of a respective channel signal in the input signal.

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